semiconductor chip, sealed with a sealing resin, and outer leads extending successively from the inner leads and protruding outwardly from the sealing resin.

2. (Amended) The semiconductor package of Claim 1, including standard inner leads and metal wires connecting tips of the standard inner leads to electrode pads on the semiconductor chip are sealed with the sealing resin, and wherein

outer leads extending successively from the standard inner leads protrude outwardly from the sealing resin, and

the LOC inner leads and the standard inner leads are co-planar.

3. (Amended) The semiconductor package of claim 1, wherein a clearance between the LOC inner leads and the die pad is larger than total thickness of the semiconductor chip and the die bond material.

4. (Amended) The semiconductor package of claim 2, wherein the LOC inner leads and the standard inner leads are both arranged along at least one side of the semiconductor chip.

5. (Amended) The semiconductor package of claim 2, wherein the LOC inner leads are arranged along a first side of the semiconductor chip and the standard inner leads are arranged along a second side of the semiconductor chip.

6. (Amended) The semiconductor package of claim 1, wherein a distance between upper surfaces of the outer leads and an upper surface of the sealing resin is different from a distance between lower surfaces of the outer leads and a lower surface of the sealing resin, and ends of the die pad are exposed at opposed side surfaces of the sealing resin and lie in a plane parallel to a plane in which the outer leads protrude.

7. (Amended) A semiconductor package including at least a semiconductor chip, metal wires, lead-on-chip (LOC) inner leads having tips spaced from and extending over

the semiconductor chip, and standard inner leads having tips arranged outside of a periphery of the semiconductor chip sealed with a sealing resin, wherein

the semiconductor chip has distributed electrode pads distributed and arranged on an upper surface of the semiconductor chip and has at least either central electrode pads rectilinearly located in a central region of the semiconductor chip or peripheral electrode pads located along the periphery of the semiconductor chip, and

the LOC inner leads and the standard inner leads are co-planar and both arranged along one side of the semiconductor chip.

8. (Amended) A method of manufacturing a semiconductor package comprising:

forming a die pad frame with a die pad surrounded by a first frame,

displacing the die pad relative to the first frame,

bonding a semiconductor chip to the die pad with a die bond material,

superposing a lead frame, including inner leads surrounded by a second frame, on the die pad frame with the semiconductor chip disposed between the die pad and the inner leads,

welding the first frame and the second frame of the lead frame together,

sealing the die pad, the semiconductor chip, and the inner leads in a sealing resin, and

removing the first frame and the second frame.

IN THE ABSTRACT:

Replace the Abstract with:

Abstract of the Disclosure

A semiconductor package includes a semiconductor chip, a die pad, an adhesive, metal wires, LOC inner leads, and standard inner leads sealed within a sealing resin. The LOC inner leads and the standard inner leads are arranged in the same plane and both are arranged along one side of the semiconductor chip. Clearance between the inner leads and the die pad larger than the total thickness of the semiconductor chip and the bonding material. Thus, a semiconductor chip having

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electrode pads broadly distributed can be employed and the section modulus of the semiconductor package can be increased.